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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/776,103 | 02/11/2004 | Kim C. Hardee | UMI-355 | 2833 |

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| EXAMINER | |
|---|---|
| HOANG, HUAN | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2827 | |

DATE MAILED: 11/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/776,103 | HARDEE, KIM C. | |
| | Examiner | Art Unit | |
| | Huan Hoang | 2827 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-35 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 21-35 is/are allowed.

6)☒ Claim(s) 1-11 and 14-20 is/are rejected.

7)☒ Claim(s) 12.13 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 043004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Claims 12, 13, 14, 15 and 17 are objected to because of the following informalities:

The word "an" in "an Standby Mode" (claim 12, line 2) and "an Sleep Mode" (claim 14, line 2) should be "a".

The word "nodes" in "said first and second voltage nodes respectively." (claim 17, lines 4-5) should be "sources". Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1-11, 14-20 are rejected under 35 U.S.C. 102(a) as being anticipated by admitted prior art.

Regarding claims 1-11, 14-16 and 18-20, the admitted prior art (Fig. 1) shows the following:

at least one sense amplifier having Active, Standby and Sleep modes thereof coupled to complementary bit lines (BL, BLB), said sense amplifier having first and second voltage nodes (118 and 124);

a first transistor (120) coupling said first voltage node to a first voltage source (VCC), a control terminal of said first transistor being coupled to receive a first control signal;

a second transistor (126) coupling said second voltage node to a second voltage source (ground), a control terminal of said second transistor being coupled to receive a second control signal;

wherein said first and second transistors comprise drive/power-gating devices;

wherein said first transistor comprises a P-channel device (120) and said second transistor comprises an N-channel device (122);

wherein said at least one sense amplifier comprises a latch circuit comprising CMOS inverters (104, 106, 108 and 110);

wherein said first voltage source comprises a supply voltage source (VCC) and said reference voltage source comprises VSS (ground);

wherein, in an Active Mode of operation, said first control signal is substantially at a level of said second voltage source (-0.3V) and said second control signal is substantially at a level of said first voltage source (VCC + 0.3V);

wherein, in a Sleep Mode of operation, said first control signal is substantially at a level greater than said first voltage source (VCC + 0.3V) and said second control signal is substantially at a level lower than said second voltage source (–0.3V).

The latch P-channel signal and the latch N-channel signal in claim 9 are considered the signals applied to transistors 120 and 126, respectively.

Fig. 3 of the admitted prior art shows a method having all the steps as recited in claims 16, 17, 19 and 20 as follows:

providing first and second transistors (316 and 320) for coupling first and second voltage nodes (LP and LN) respectively of said sense amplifier to respective first and second voltage sources (VCC and ground);

enabling said first and second transistors in an Active Mode of operation to couple said first and second voltage nodes to said first and second voltage sources respectively;

disabling said first and second transistors in a Standby Mode of operation to decouple said first and second voltage nodes from said first and second voltage sources respectively;

wherein said step of enabling said first and second transistors is carried out by applying a voltage substantially equal to a level of said second voltage source to a control terminal of said first transistor and a voltage substantially equal to a level of said first voltage source to a control terminal of said second transistor (Active, LPB = 0V and LNB =VCC);

wherein said step of disabling said first and second transistors is carried out by applying a voltage substantially equal to a level of said first voltage source to a control terminal of said first transistor and a voltage substantially equal to a level of said second voltage source to a control terminal of said second transistor (STBY, LPB = VCC and LNB = 0V).

***Allowable Subject Matter***

4. Claims 22-35 are allowed.

5. Claims 12 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art does not teach or suggest the following:

wherein, in an Active Mode of operation, said first control signal is substantially at a level of said second voltage source and said second control signal is substantially at a level of said first voltage source.

wherein said LPB and said LNB signals present Active, Standby and Sleep states thereof.

disabling said first and second transistors in a Standby Mode of operation to decouple said first and second shared voltage nodes from said first and second voltage nodes respectively; and further disabling said first and second transistors in a Sleep Mode of operation by applying a voltage greater than that of said first voltage source to a control terminal of said first transistor and a voltage less than that of said second voltage source to a control terminal of said second transistor.

wherein said first and said second signals present Active, Standby and Sleep states thereof.

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Arimoto et al. discloses a dynamic semiconductor memory device capable of rearranging data storage from a one bit/one cell scheme in a normal mode to a one bit/two cell scheme in a twin-cell mode for lengthening a refresh interval.

Ooishi discloses a semiconductor memory device with a voltage down converter stably generating an internal down-converter voltage.

7. .Any inquiry concerning this communication or earlier communications from the examiner should be directed to Huan Hoang whose telephone number is (571) 272-1779. The examiner can normally be reached on Mon-Fri 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Huan Hoang
Primary Examiner
Art Unit 2827

HH
11/8/05